CLAIMS:

1. (Currently amended) An uninterruptible power supply comprising:

a controlled rectifier having an input coupled to receive AC power and an output coupled to a DC bus;

a battery coupled to the DC bus;

an inverter having an input coupled to the DC bus and an output coupled to a load; and

a control system coupled to the controlled rectifier and the inverter, the control system comprising three microprocessors, wherein a first microprocessor functions as an overall controller, a second microprocessor controls the rectifier, and a third microprocessor controls the inverter;

wherein the three microprocessors communicate via a common global memory.

2. (Canceled)

3. (Currently amended) The uninterruptible power supply of ~~claim 2~~ **claim 1** further comprising a memory arbitration circuit including a complex programmable logic device programmed to allow priority-driven, non-preemptive access by the microprocessors to the common global memory.

4. (Original) The uninterruptible power supply of claim 1 comprising a plurality of components interconnected by a peer-to-peer controller area network, wherein the network accommodates fragmented messaging.

5. (Original) The uninterruptible power supply of claim 1 further comprising a battery current monitoring circuit comprising:

a current sensor disposed to monitor the battery current;

a first amplifier circuit receiving an output from the current sensor corresponding to discharging battery current, amplifying it by a first factor, and outputting it to the control system;

a second amplifier circuit receiving an output from the current sensor corresponding to a charging battery current, amplifying it by a second factor greater than the first factor, and outputting it to the control system;

wherein the control system selects as its input the output of the first amplifier when the battery is discharging and the output of the second amplifier circuit when the battery is charging.

6. (Original) The UPS of claim 1 having a three-phase input and independent zero-crossing detection circuits for each input phase, wherein the second microprocessor independently determines a phase shift introduced by each zero cross detection circuit and adjusts the firing signal timing for each rectifier phase to negate the phase shift.

7. (Original) The UPS of claim 6 wherein the second microprocessor is configured to change the firing sequence of the rectifier to compensate for a phase rotation of the three-phase input.

8. (Original) The UPS of claim 6 wherein the second microprocessor qualifies the input voltage by measuring the voltage on a first phase of said three-phase input, the frequency on a second phase of said three-phase input, and the phase sequence between either said first phase or said second phase and a third phase of said three-phase input.

9. (Currently amended) The UPS of claim 1 wherein the second microprocessor implements a phase lock loop for synchronizing rectifier firing, wherein the phase lock loop includes a finite impulse response filter on the input voltages~~, thereby~~ **for** removing low frequency harmonics from the input signal.

10. (Original) The UPS of claim 1 wherein the third microprocessor implements a nested control loop having an inner loop and outer loop, said inner loop regulating inverter current using a discrete sliding mode controller, and said outer loop regulating the inverter voltage using a harmonic servomechanism controller.

11. (Currently amended) A method of controlling the output current of a controlled rectifier having its output connected to a DC bus with a battery coupled thereto, the method comprising:

sensing the DC bus voltage;

comparing the sensed voltage to a voltage setpoint;

adjusts the firing signal timing ~~increasing or decreasing the rectifier firing angle~~ to minimize a difference between the sensed voltage and the voltage setpoint;

determining whether an input current of the rectifier or a charging current of the battery is above a predetermined limit; and

switching control to a different control loop to maintain the input current or the charging current within the predetermined limit.

12. (Currently amended) The method of claim 11 wherein the step of switching to a different control loop includes ~~pre-loading the integrator~~ **setting the value of an integrator element** of the different control loop **to a predetermined level** to prevent a discontinuity in an output of the different control loop.

13. (Original) The method of claim 11 wherein the different control loop includes a non-linear element.

14. (Original) The method of claim 11, wherein on starting the rectifier, the voltage setpoint is gradually increased from an initial value to a final value.

15. (Currently amended) The method of claim 11 wherein the voltage setpoint is selected to cause a ~~particular~~ **desired** charging current to flow into said battery.

16. (Original) The method of claim 15 wherein the voltage setpoint is selected from one of a higher value to accomplish faster charging or a lower value to accomplish slower charging.

17. (Original) The method of claim 15 wherein the voltage setpoint is selected to cause zero charging current to flow into said battery.

18. (Original) The method of claim 15 wherein the voltage setpoint is selected as a function of battery temperature.

19. (Original) A method of operating a plurality of uninterruptible power supplies in parallel comprising:

adjusting a phase angle of a voltage generated by each uninterruptible power supply to eliminate real power unbalances among the plurality of uninterruptible power supplies;

adjusting a magnitude of a voltage generated by each uninterruptible power supply to eliminate reactive power unbalances among the plurality of uninterruptible power supplies; and

shifting a location of a harmonic servo compensator pole to reduce the bandwidth of the controller for each harmonic.

20. (New) An uninterruptible power supply comprising:

a controlled rectifier having an input coupled to receive AC power and an output coupled to a DC bus;

a battery coupled to the DC bus;

an inverter having an input coupled to the DC bus and an output coupled to a load; and

a control system coupled to the controlled rectifier and the inverter, the control system comprising three microprocessors, wherein a first microprocessor functions as an overall controller, a second microprocessor controls the rectifier, and a third microprocessor controls the inverter; and

a plurality of components interconnected by a peer-to-peer controller area network, wherein the network accommodates fragmented messaging.

21. (New) An uninterruptible power supply comprising:

a controlled rectifier having an input coupled to receive AC power and an output coupled to a DC bus;

a battery coupled to the DC bus;

an inverter having an input coupled to the DC bus and an output coupled to a load; and

a control system coupled to the controlled rectifier and the inverter, the control system comprising three microprocessors, wherein a first microprocessor functions as an overall controller, a second microprocessor controls the rectifier, and a third microprocessor controls the inverter;

a three-phase input and independent zero-crossing detection circuits for each input phase, wherein the second microprocessor independently determines a phase shift introduced by each zero cross detection circuit and adjusts the firing signal timing for each rectifier phase to negate the phase shift; and

wherein the second microprocessor is configured to change the firing sequence of the rectifier to compensate for a phase rotation of the three-phase input.

22. (New) An uninterruptible power supply comprising:

a controlled rectifier having an input coupled to receive AC power and an output coupled to a DC bus;

a battery coupled to the DC bus;

an inverter having an input coupled to the DC bus and an output coupled to a load; and

a control system coupled to the controlled rectifier and the inverter, the control system comprising three microprocessors, wherein a first microprocessor functions as an overall controller, a second microprocessor controls the rectifier, and a third microprocessor controls the inverter;

a three-phase input and independent zero-crossing detection circuits for each input phase, wherein the second microprocessor independently determines a phase shift introduced by each zero cross detection circuit and adjusts the firing signal timing for each rectifier phase to negate the phase shift; and

wherein the second microprocessor qualifies the input voltage by measuring the voltage on a first phase of said three-phase input, the frequency on a second phase of said three-phase input, and the phase sequence between either said first phase or said second phase and a third phase of said three-phase input.